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Semiconductor Measurement Technology:

Microelectronic Processing Laboratory at NBS

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ABSTRACT

This report describes the facilities and processes used at NBS for the fabrication of *npn* silicon transistors in support of the Electron Devices Division's program in process control and measurement technology. The description of the processes includes details of techniques used for contamination control and the various steps required for the preparation of planar silicon transistors. A description of the electrical properties of the devices is also presented.

Key Words: Diffusion; metallization; oxidation; photolithography; silicon; transistors.

1. INTRODUCTION

The purpose of this report is to describe the processes and facilities used in the fabrication of microelectronic test structures which are an integral part of specific test methods being developed for use in the semiconductor industry. The Microelectronic Processing Laboratory is located in the Electron Devices Division at the National Bureau of Standards. The facility is low-cost in nature, but careful layout of its components has allowed the fabrication of both bipolar and MOS test structures of high quality.

The need for a processing facility at NBS follows from the requirement that the effective development of various measurement procedures demands a thorough knowledge and control of the processes used in the fabrication of test structures. The facility allows the flexibility to perturb the fabrication process so as to study the limits of measurement methods as influenced by processing variations. Additionally, the availability of a processing laboratory allows the development of new test structures and permits the introduction of specific contaminants in controlled amounts during the processing sequence. The result is a general purpose laboratory devoted to monolithic silicon processing. The laboratory has the capability of producing certain specialized microelectronic devices starting with single crystal ingots of silicon and finishing with a hermetically sealed unit. To date, both bulk *npn* and *pnp* transistors

have been fabricated in addition to *p*-channel and complementary MOS devices.

To illustrate the basic facilities and technology available in the processing laboratory, the basic processing steps required for a bipolar *npn* process will be described. This bipolar process consists of four photolithographic steps, three thermal oxidation steps, two diffusion steps, and a metallization step. However, additional capabilities exist in the laboratory for the production of other device technologies. For example, in the production of MOS devices, facilities are available for the growth of dry oxides and the deposition of polysilicon layers. An epitaxial reactor is available for the deposition of layers of silicon of various thicknesses and resistivity as may be required for junction-isolated integrated circuits. Additionally, equipment is available for die and wire bonding operations and for packaging of the devices in hermetic packages.

The next section of this report is concerned with contamination control. The understanding of contamination control as applied to microelectronic manufacturing is essential because of the interaction of contamination with device performance. The electrical properties of silicon devices may be drastically altered by contamination introduced during the various processing steps. A sensitive measure of the presence of contaminants is the degradation of such electrical parameters as leakage current or breakdown voltage of a bipolar device.

The photolithography, thermal oxidation, diffusion, and metallization steps are described in succeeding sections. By repeating the oxidation, photolithography, and diffusion steps, the impurity distribution in the semiconductor material may be modified to attain specific junction dopant profiles. In the final section, specific parameters, such as times, temperatures, and flow rates, are given for a typical *npn* transistor process.

2. CONTAMINATION CONTROL

2.1 Facilities for Contamination Control

A primary objective of the NBS Microelectronic Processing Laboratory is to produce semiconductor devices with well-defined and predictable electrical characteristics. This goal requires minimal introduction of contamination into the process. Four major sources of contamination in semiconductor processing are airborne particles, impurities in the water used for the processing, contamination present in gases used in the oxidation and diffusion of wafers, and surface contamination on the silicon wafers. Each of these sources of contamination is discussed in the following paragraphs.

To assure that the silicon wafers are not subjected to airborne contamination, all chemical operations, diffusions, oxidations, and metallizations are performed in nearly particle-free environments. Figure 1

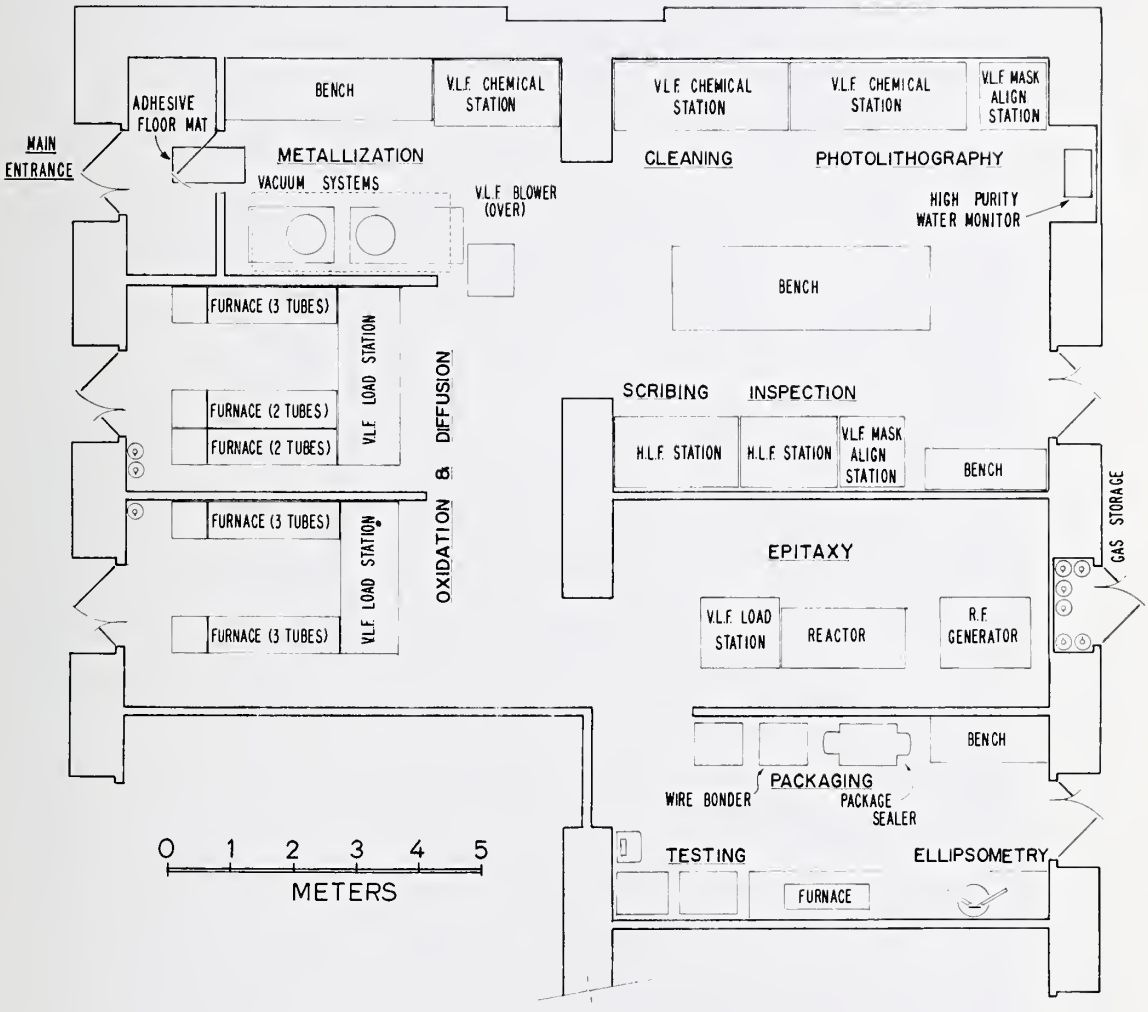


Figure 1. The floor plan of the Microelectronic Processing Laboratory at the National Bureau of Standards.

shows the general floor plan of the laboratory. Laminar flow stations are included at all locations where wafers are handled. These stations are designated as being either vertical laminar flow (V.L.F.) or horizontal laminar flow (H.L.F.) stations. Airborne contamination consists principally of particulates which range in size from 0.5 to 20 μm. Particles larger than 20 μm tend to settle out rapidly and are small in number. Particles smaller than 0.5 μm tend to coagulate and become relatively few in number. Control of the number of particles in a work space is accomplished with air blowers, followed by high efficiency particulate air filters. Proper design and adjustment of blower and filter systems result in a laminar air flow that excludes the room air from the work space.

Figure 2 shows a typical H.L.F. station. Local laminar flow stations are relatively low-cost alternatives to controlling the contamination in the entire room. The performance of such units is measured at least every six months to assure the integrity of the filter systems. Airflow velocity normal to the air filter exit is maintained at 27.5 m/min within ±20 percent across the entire area of the exit. Additionally, the number and size of particles are determined with a light scattering particle counter [1].* Each of the laminar flow stations is required to have a particle count not to exceed 3.5 particles of size 0.5 μm and larger per liter of air. This corresponds to Class 100 contamination control [2]. Outside the load stations, the particle count is normally 10 to 100 times greater. A positive air pressure is not maintained between the facility and the surrounding hallways. Entrance to the facility is allowed from the main entrance. Four other doors are provided for emergency purposes. Particles are removed from shoes by an adhesive-coated mat placed at the main entrance; however, personnel working within the facility are not required to wear special clothing. Wafers are placed in protective containers for transportation between laminar flow stations.

High purity water is used in solutions for cleaning wafers and processing materials and for rinsing operations. Tap water is first filtered to remove particulate matter, passed through a water softener, and then subjected to a reverse osmosis purification process which rejects approximately 99 percent of the mineral content. Next, carbon filters reduce the remaining soluble organics, and finally traces of dissolved minerals are removed by two deionization columns. In these columns, a cation exchanger replaces metallic cations by hydrogen ions and an anion exchanger removes silica. The water is then stored in a 3800-L fiberglass tank prior to its delivery to a recirculating loop and to its point of use. Included in the recirculating system are two additional mixed bed deionization columns, an ultraviolet lamp for microbial control, and filters for particle removal.

The system will produce 160 L of water per hour with a 3500-L reserve. The resistivity, which is continuously monitored, is typically 16 to 18 MΩ•cm; the number of biologically active organisms is less than 10 per cubic centimeter; and the total electrolyte content (as NaCl) is

*Figures in brackets indicate references at the end of this report.

Figure 2. Typical horizontal laminar flow stations used for the inspection of silicon wafers and for the final assembly operations.

less than 100 parts per billion by weight. The water meets the ASTM specification for Type 1 Reagent Water [3].

High purity compressed gases are used in the oxidation and diffusion operations. Nitrogen is obtained from a 5700-L liquid source equipped with a vaporizer. All other gases are obtained in cylinders from commercial suppliers as "Electronic Grade" products. Moisture in both the nitrogen and oxygen is controlled with molecular sieve desiccants in gas driers with automatic reactivation provisions. Typical moisture contents are less than 5 parts per million by volume. Absolute 0.22-μm filters are provided at point of use to exclude particles in the process stream. All process gases are distributed to their points of use in the laboratory in stainless steel tubing.

2.2 Wafer Cleaning

The reproducibility and stability of solid state devices depend, in part, on the ability to minimize contamination on their surfaces during fabrication. Typically, contaminants on silicon wafers fall into three categories. The first includes organic molecules such as oils, waxes, and greases that contaminate wafers from the room air, plastic containers, and photochemicals. The second class of contaminants is atomic in nature and includes metallic ions which can be chemically bonded to the silicon surface. Metallic ions can originate from wafer polishing operations and affect the carrier lifetime and trapping characteristics of the silicon. The third type of contaminant is comprised of particles attached to the silicon surface. These particles are frequently micrometer- and submicrometer-sized particles of the silicon wafer itself generated during polishing operations. Attached particles can cause pinholes in oxide layers and can be detrimental to the photomasking processes. Particles are removed from the surfaces first.

The particulate matter is removed by ultrasonic cleaning using a wetting agent in water at 82 ± 3°C. The wetting agent, in the form of a highly dilute nonionic detergent, inhibits the reattachment of the particles to the surface once they have been dislodged by the cavitation of the liquid. The temperature of the water is important since it influences the vapor pressure, viscosity, and the surface tension of the water. In turn, these properties influence the cleaning efficiency of water used in the ultrasonic cleaner. The ultrasonic cleaning tank has an overflow feature to prevent particles from reattaching to the cleaned wafers when they are removed from the tank. The efficiency of an ultrasonic cleaning routine may be evaluated by using dark field microscopy to count the number of particles adhering on silicon surfaces at 100X magnification both before and after cleaning [4].

Two solutions are used sequentially to remove both the organic and metallic contaminants remaining on the particle-free wafers. These solutions are based on the properties of hydrogen peroxide solutions at high and low pH [5]. The first solution consists of equal parts of hydrogen peroxide (30 percent, unstabilized) and ammonium hydroxide (27 percent) added to two parts of high purity water. The wafers are placed

into the solution and heated to 40°C for 20 min. The second solution consists of equal parts of hydrogen peroxide (30 percent, unstabilized) and hydrochloric acid (37 percent) added to two parts of high purity water. Again, the wafers are placed into this solution and heated to 40°C for 20 min. Caution should be exercised when working with these solutions as both are strong oxidizers and can evolve large quantities of gas even when cold. Both solutions are mixed just prior to use and disposed of into a chemically resistant drain immediately after use. Between each step of the cleaning process, the wafers are washed in an overflow wash tank with a nitrogen burst agitation at a water flow rate of 40 L/min for a period of 10 min. Such a washing procedure has proven sufficient to provide a final rinse water effluent with a resistivity greater than 10 MΩ•cm. The wafers are centrifugally spun dry in filtered nitrogen. This cleaning process is used before each diffusion, oxidation, or metallization step.

3. PHOTOLITHOGRAPHY

The photolithographic processes define the geometries of the semiconductor elements and consist of the five basic steps illustrated in figure 3. First, a photosensitive lacquer or photoresist is applied to the surface to be etched; in the NBS facility, positive photoresist is used. Positive photoresists are characterized by the fact that where exposed to ultraviolet light they are rendered soluble in developer. The excess photoresist is removed by spinning the wafer at 4000 revolutions per minute for 15 s at room temperature. The resulting film is prebaked in an oven purged with nitrogen at 75°C for 20 min. Second, the photoresist is exposed with an ultraviolet light through a patterned photomask in intimate contact with the wafer. Precise registration of the pattern with the pattern(s) introduced in earlier steps is made possible with a mask alignment machine. Third, the pattern is developed by agitating the wafer in a nonmetallic developer for 20 s at room temperature. The photoresist application, exposure, and development are performed in an area free of ultraviolet light. Yellow fluorescent lamps have a sufficiently low level of ultraviolet radiation. This area is designated as the photolithography section of the laboratory as shown on the floor plan in figure 1. The development process removes the photoresist in those areas where it is desired to etch the underlying layer. The film is then baked at 120°C for 20 min in a nitrogen ambient to improve the etch resistance and adhesion. Fourth, the layer of interest is patterned by an appropriate etchant. Buffered hydrofluoric acid is used to etch oxide layers, and a phosphoric acid is used to define aluminum metallization patterns. The composition of each of the etchants used in this process is as follows:

Buffered Hydrofluoric Acid Etchant	
Ammonium fluoride	389 g
Hydrofluoric Acid (48 percent)	140 mL
Deionized water	1 L

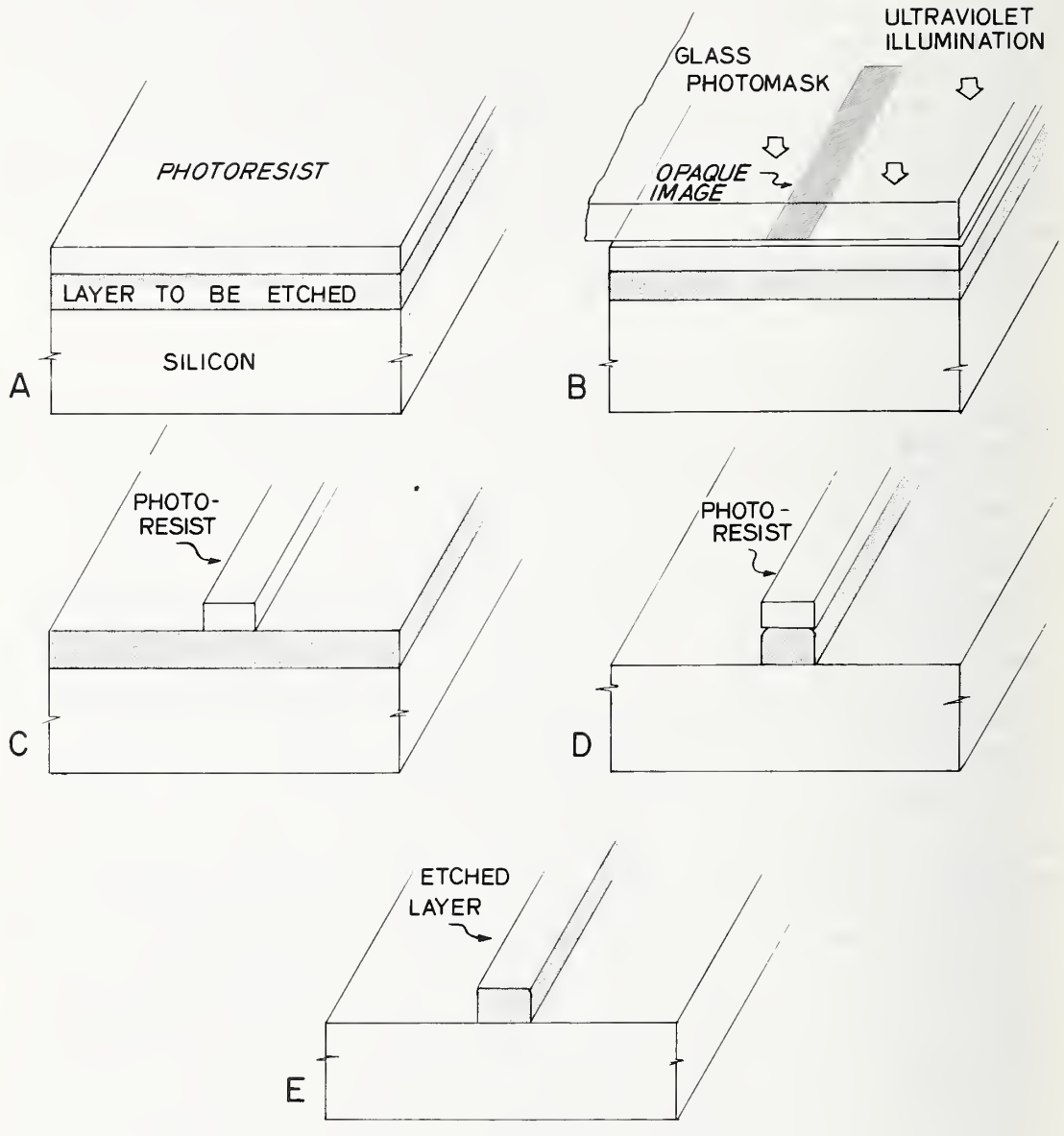


Figure 3. The sequence of operations in a positive photolithographic process. A) The photoresist is applied to the layer to be etched. B) The photoresist is exposed through a patterned glass photomask with ultraviolet light. C) The exposed photoresist image is developed, removing the exposed resist. D) The layer to be etched is removed by a suitable etchant. E) The photoresist is removed with solvents leaving the etched layer.

Aluminum Metallization Etchant

Phosphoric acid (85 percent)	1 L
Nitric acid (70 percent)	50 mL
Deionized water	250 mL

Note: All chemicals used in the preparation of these etchants are Electronic Grade.

Finally, the remaining photoresist is dissolved and removed with acetone. This is followed by the previously described cleaning procedure to remove all traces of the photoresist.

The facilities for the photoresist spinning, exposure, and chemical etching operations are shown in figure 4. Many of the important parameters of the photolithographic process are controlled to a high degree. For example, the illumination level of the ultraviolet light is continuously monitored during the photoresist exposure by a photosensor integral with the mask alignment machine to provide compensation for the aging of the exposure lamp by varying the exposure time. The angular velocity and acceleration of the wafer during photoresist spinning is also controlled. These facilities and the above procedures are capable of producing device structures with minimum line width of 0.25 mil (6.4 μm).

All lots of photoresist are sampled and tested to assure that the viscosity and solids content of the emulsion conform to the manufacturer's specifications [6]. Resist with a nominal viscosity of 5 centipoise and a solids content of 35 percent is used for all oxide and metallization photolithography.

4. THERMAL OXIDATION

In many of the processing sequences being discussed here, thermally grown silicon dioxide is used to mask the various diffusions. The thickness of the silicon dioxide films grown in an oxidizing atmosphere depends on the time, temperature, and water vapor content of the oxidizing atmosphere.

Two different systems are used for the growth of silicon dioxide. Both are shown schematically in figure 5. The pyrogenic system [7] shown in figure 5a uses hydrogen, oxygen, and nitrogen. The system has provision for measuring and controlling the flows of each gas to a quartz burner or "injector" located at one end of the quartz oxidation tube. To grow an oxide in an ambient of water vapor, the hydrogen and oxygen are permitted to flow to the injector. The temperature of the oxidation tube at the exit of the injector is kept at approximately 500°C. This is sufficiently high to assure the autocombustion of the gases to form a controlled amount of water vapor. Flow, pressure, and temperature interlocks assure that the system can only be operated in a safe condition. Dry nitrogen can also be admitted to the quartz tube, in the absence of oxygen and hydrogen, to permit the tube to be used as a dif-

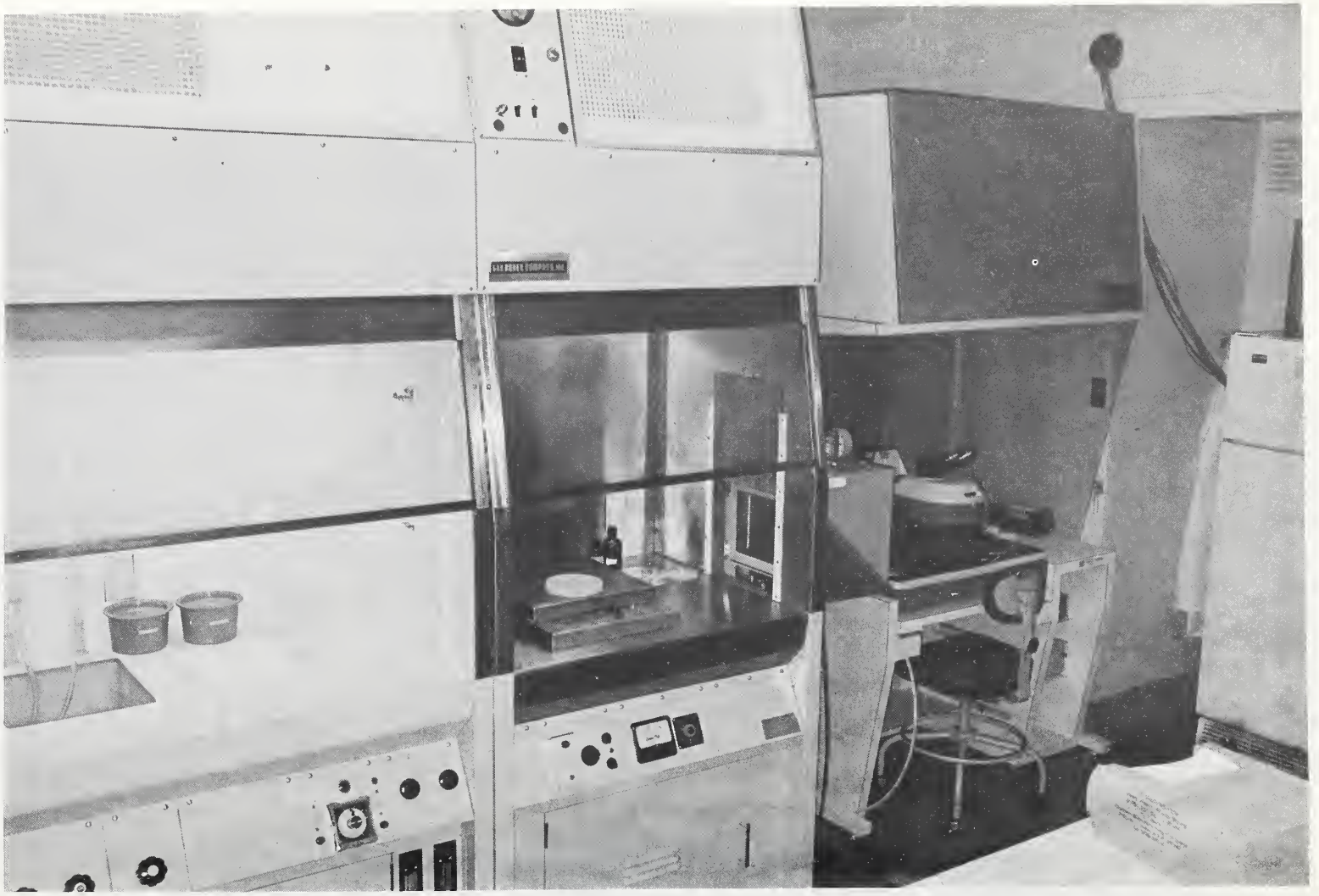
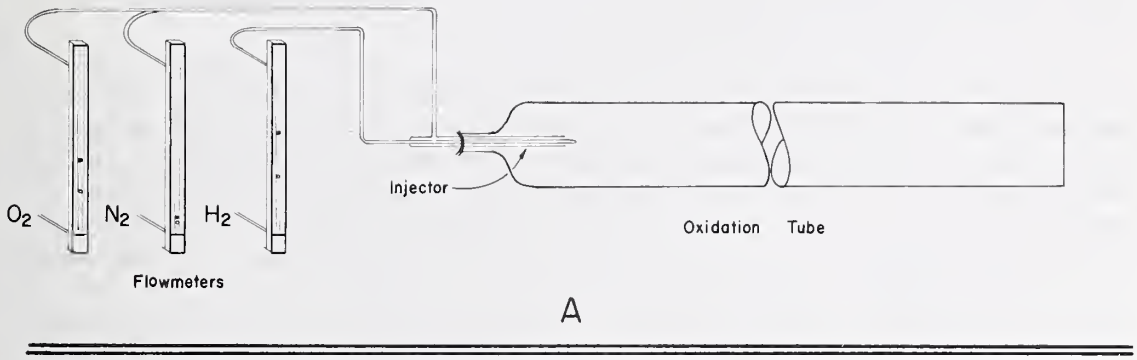


Figure 4. A view of the laminar flow stations used in the photolithographic operations. On the left is the area used for the development and etching operations. The middle station is for the application of photoresist. The mask aligner and exposure apparatus are shown on the right.



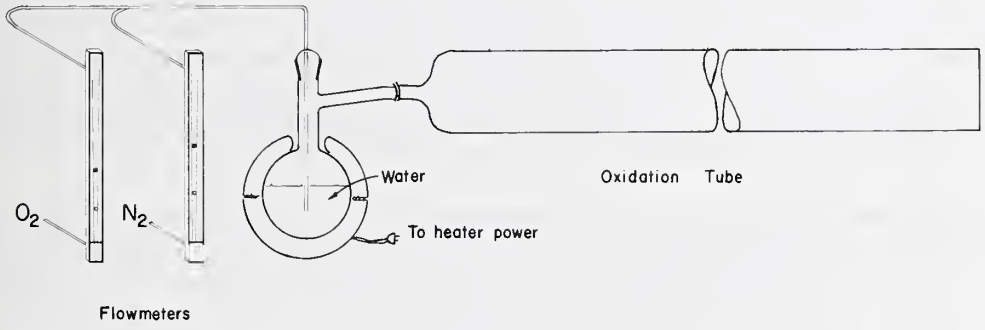


Figure 5. The two systems used for the growth of thermal oxides on silicon. A) A pyrogenic system using the reaction of hydrogen and oxygen for the production of water vapor, and B) a steam generation system employing a quartz boiler and heating jacket.

fusion tube. By heating silicon wafers that have a diffused layer on their surface, the junction depth and surface concentration of the diffusion can be changed. Additionally, a dry nitrogen annealing of the grown oxide layer decreases its hydroxyl content and improves the ability of the photoresist to adhere to the oxide for the subsequent photolithographic process. The annealing of oxide layers after growth has been shown to decrease the fixed charge [8] with an improvement of the junction leakage characteristics.

The second system for oxidation, shown in figure 5b, consists of a heated flask containing high purity water for the generation of steam. The steam, with an oxygen or nitrogen gas carrier, is admitted to the quartz oxidation tube. In this system, the concentration of water in the vapor phase is higher than in the pyrogenic system. This results in approximately a 20-percent increase in the growth rate of the oxide at a given temperature. Although simpler in design, it suffers the disadvantage of having higher possible contamination in the oxide films as a result of residual impurities in the high purity water used in the steam generator. It is necessary to incline the quartz connecting tube to assure that no droplets of water are transferred from the steam generator to the oxidation tube.

In both oxidation systems, wafers are placed vertically in quartz boats for the oxidation. The wafer spacing is 4 mm and the orientation is edgewise to the direction of gas flowing in the oxidation tube. Oxidation tubes are constructed of fused silica, 80 mm in diameter with a 2-mm wall thickness. The temperature of the quartz tube is measured with thermocouples as described in the next section.

The thickness and the index of refraction of the oxide films are determined with ellipsometry [9]. The thickness of layers in the range of 50 to 100 nm can be determined to an accuracy of better than 5 nm.

5. DIFFUSION

Phosphorus and boron depositions and their associated drive-in steps are required to form an *npn* transistor. For both dopants, commercially available solid diffusion sources are used. These solid sources provide some attractive alternatives to gaseous or liquid sources. In a properly controlled diffusion system, there is nearly equal mass transfer to all silicon surfaces resulting in greater uniformity of sheet resistance across the wafer. The complexity of the gas connections to the furnace is reduced, and the need to handle toxic and corrosive gases is eliminated.

Boron nitride is used as the boron source in the base diffusion. The composition of the boron nitride, as determined by spectroscopic analysis, is [10]:

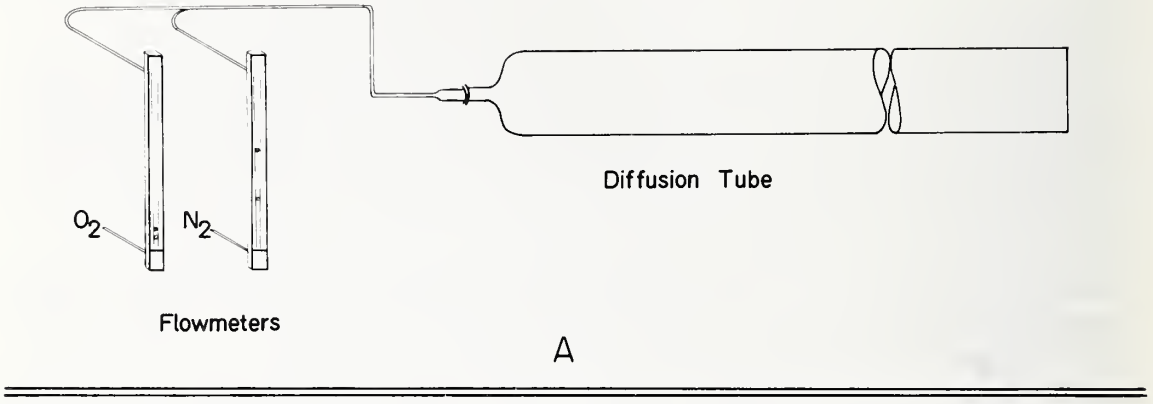
Boron	41.5 percent
Nitrogen	52.0
Oxygen	4.0 - 6.0
Carbon	less than 0.05
Calcium	0.20
Chloride	0.10
Other	0.20

The boron nitride wafers, as obtained from the manufacturer, are degreased in trichloroethylene at 60°C for 5 min followed by a 40°C soak in acetone for 3 min. The wafers are then washed in high purity water for 5 min, etched in hydrofluoric acid (48 percent) at room temperature for 1 min, and washed again until the rinse water reaches a resistivity of 10 MΩ·cm. The wafers are then dried at 345°C for 30 min in nitrogen. The surface of the boron nitride is then converted to a boron glass which acts as the source of boron dopant. This is accomplished in the same furnace which is used for the boron diffusions. The wafers are activated at a temperature of 965°C for 30 min in an oxygen ambient with a flow rate of 0.5 L/min. After this procedure, the silicon wafers are placed vertically between the boron nitride wafers with the oxide-masked sides of the silicon wafers facing the boron nitride wafers. During the diffusion, the nitrogen flow in the tube is adjusted to 0.5 L/min and is directed normally to the faces of the wafers. The boron glass on the surfaces of the boron nitride wafers effects a mass transfer to the surfaces of the silicon wafers during the diffusion. The boron glass on the source wafers evaporates over many diffusion runs. The boron nitride wafers are reactivated when more than a 10-percent change in the run-to-run sheet resistance is noted.

For 50-mm (2-in.) diameter silicon wafers, the boron nitride wafers are approximately 60 mm in diameter and 1 mm thick. The wafer spacing is maintained at 2 mm by slots in the quartz diffusion boat.

N-type diffusions for the emitter deposition employ a solid source composed of 25-percent silicon pyrophosphates and 75-percent inert binder. The pyrophosphate diffusion source wafers require no wet chemical cleaning, but they are prefired for 30 min in nitrogen at 1025°C. Care must be exercised in handling the phosphorus wafers as they exhibit a 0.6-percent thermal expansion coefficient between room temperature and 1025°C. For 50-mm diameter wafers, a 0.5-mm allowance in diameter for expansion of the wafers in the quartz diffusion boat must be provided to prevent deformation or breakage. The technique for performing the *n*-type diffusion is nearly the same as that for the *p*-type diffusion. Wafers are loaded vertically into the quartz boat with their oxide-masked sides facing the solid sources. The silicon wafer and source spacing is maintained at 2 mm by the slots in the boat. Nitrogen is admitted to the tube and its direction of flow is normal to the faces of the wafers.

Figure 6a shows the manner that the process gases are admitted to the diffusion tube for both the *n*-type and *p*-type diffusions using solid



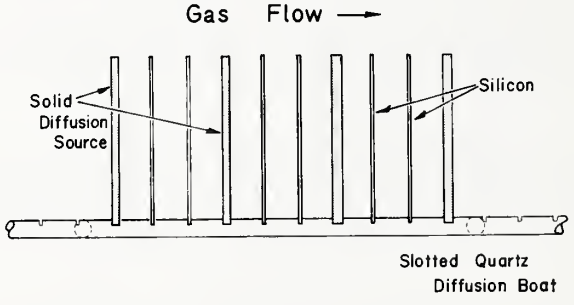


Figure 6. A diffusion system employing solid dopant sources. A) The flow of either nitrogen or oxygen to the diffusion tube may be controlled by flowmeters in the gas lines. B) The sequence of silicon wafers and solid source wafers in the two-rail quartz diffusion boat is shown.

sources. Figure 6b shows the manner in which source wafers and silicon wafers are placed into a quartz boat prior to the diffusion.

Temperatures of both the diffusion and oxidation tubes are measured with platinum versus platinum-10% rhodium thermocouples (ANSI Type S) [11]. The electrical potential developed across the thermocouple is converted to an equivalent temperature by a digital thermometer and displayed. The overall system has a resolution of 0.1°C and a claimed accuracy of ±0.5°C. The length of the hot zone of the furnace is 90 cm and has at worst a 0.2°C temperature difference along the length of a 20-cm quartz boat.

Two other measurements are routinely performed to assure the consistency of the diffusion processes. Junction depth is measured by exposing the diffused layers with a cylindrical groove in the surface of the silicon [12]. The junctions are then delineated with chemical stains [13]. The junction depth is calculated knowing the width and the radius of curvature of the groove and the width of the stained region. These measurements are made using a calibrated filar ocular on a brightfield microscope. The sheet resistance of the diffusions is measured with the four-probe technique. This system consists of a collinear four-probe array, a constant current source, and a millivoltmeter. The voltage-to-current ratio multiplied by the appropriate scale factor gives the sheet resistance of the diffused layer [14].

6. METALLIZATION

An evaporated layer of 99.999-percent aluminum 800 ± 40 nm thick is used to contact the silicon devices and to provide interconnections between various diffused regions of the wafer. Figure 7 is a photograph of the electron beam deposition system used for depositing the layer. The system consists of an oil-pumped vacuum system with an ultimate pressure of less than 1×10^{-6} Pa (1×10^{-8} torr). The aluminum is evaporated by the heat generated by a focused beam of electrons striking a water-cooled copper crucible of aluminum. Typically, the electron beam current is 400 mA at an accelerating potential of 10 kV. The silicon wafers are held approximately 200 mm from the center of the aluminum source. The aluminum thickness is measured by a deposition controller that measures both the rate of evaporation and the total thickness of metal deposited with the use of a quartz crystal oscillator whose frequency is a function of the aluminum thickness. Typically, aluminum is deposited at a rate of 5 nm/s on wafers at ambient temperature. The wafers are rotated in a planetary fixture that provides uniform metallization thickness over the undulating surface of the patterned silicon wafers.

The thickness of the evaporated aluminum films is measured after evaporation with a multiple-beam interferometer to assure that proper thickness has been achieved [15]. This technique has a repeatability of approximately 30 nm. Depositions are made on optically flat glass, a part of which is occluded from the evaporant with a 1-mm wire. The wire is removed and the glass overcoated with a 100-nm layer of aluminum to pro-

Figure 7. The electron beam evaporation apparatus for the deposition of aluminum. Notice the vertical laminar flow unit located over the area where wafers are handled.

vide uniform reflectance over the metallization step. The fringe pattern produced by the interferometer is photographed and the distance between the fringes measured on a toolmaker's microscope.

In order to assure a low resistance electrical contact to the back surface of the silicon wafer, antimony-doped (0.6%) gold is thermally evaporated onto this surface. The antimony-doped gold is evaporated from an alumina-coated crucible wound with 0.5-mm diameter tungsten wire. An electrical current of approximately 40 A is sufficient to heat the crucible to attain an evaporation rate of 50 nm/min. This evaporation is performed after all oxidations, diffusions, and the aluminum metallization have been completed. The vacuum system used for this evaporation is similar to that used for the aluminum deposition, and the methods used to monitor and verify the thickness of the deposition are the same.

After the evaporation of the aluminum and the gold metallizations, the wafers are placed into a furnace at 500°C. Nitrogen with a water vapor content of less than 10 parts per million is passed through the furnace tube at a flow rate of 1 L/min. The nitrogen is passed through a cold trap at 77 K immediately prior to its introduction to the furnace to remove water vapor. The purpose of this step is to microalloy the aluminum and gold metallizations into the silicon to insure the lowest possible contact resistance between the silicon and the metals.

7. *NPN* TRANSISTOR PROCESS

7.1 Typical *npn* Process

The following basic processes are used to form a typical *npn* transistor. With silicon wafers oriented in the (111) direction and having a room temperature resistivity between 5 and 10 Ω•cm, the front surfaces of the wafers are chem-mechanically polished and the back surfaces of the wafers are etched to a matte finish. Wafers are 50 mm (2 in.) in diameter and 0.35 mm (0.010 in.) thick. The bipolar transistor has a base sheet resistance of approximately 200 Ω/□ and a base junction depth of 1.8 μm. After the emitter diffusion, the effective base width is about 0.8 μm, resulting in a common-emitter current gain of about 100. Higher or lower current gains can be achieved by adjusting the processing parameters associated with the emitter diffusion. All high temperature processing steps are summarized in table 1.

7.2 Initial Silicon Dioxide Masking

7.2.1 Initial Silicon Wafer Cleaning

7.2.1.1 Ultrasonically clean wafers in water exceeding 16 MΩ•cm at 80°C for a period of 10 min. Add one part in 10,000 of a nonionic detergent to aid in the removal of attached silicon particles.

7.2.1.2 Rinse wafers in an overflow wash tank for 10 min or until the resistivity of the effluent water exceeds 14 MΩ•cm.

Table 1. High Temperature Processing Steps.

Step	Temperature, °C	Time, min	Ambient	Flow Rate, L/min
Oxidation	1100	5	Oxygen	0.8
	1100	30	Oxygen + Hydrogen	0.8 + 0.7
	1100	5	Oxygen	0.8
	1100	15	Nitrogen	1.0
Base Deposition	965	30	Nitrogen	0.5
Base Drive-in	1100	5	Oxygen	0.8
	1100	30	Oxygen + Hydrogen	0.8 + 0.7
	1100	5	Oxygen	0.8
	1100	60	Nitrogen	1.0
Emitter Deposition	1025	18	Nitrogen	0.5
Emitter Drive-in	925	30	Oxygen + Steam	1.0
	925	5	Oxygen	1.0
	925	15	Nitrogen	1.0
Microalloy	500	10	Nitrogen	1.0

7.2.1.3 Place wafers into a solution of one part ammonium hydroxide, one part hydrogen peroxide, and two parts high purity water. Heat the solution to approximately 40°C for 20 min. This cleaning solution is designed to remove any residual organic material on the surface of the wafers.

7.2.1.4 Rinse wafers in overflow wash tank for 5 min in water exceeding 16 MΩ•cm resistivity at a flow rate of 40 L/min. For this and all other rinsing procedures, it has been established that the wash times and flow rates for the wash tanks are sufficient to assure that the effluent water resistivity is greater than 10 MΩ•cm.

7.2.1.5 Dip wafers in 10-percent hydrofluoric acid solution for 10 s.

7.2.1.6 Rinse wafers in overflow wash tank for 5 min.

7.2.1.7 Place wafers in a solution of one part hydrochloric acid, one part hydrogen peroxide, and two parts deionized water. Heat the solution to approximately 40°C for 20 min. This solution is designed to remove residual metals on the surface of the wafers. Be careful of this step as the solution tends to be exothermic as it is heated.

7.2.1.8 Rinse wafers in high purity water for 10 min and spin wafers dry in a nitrogen ambient.

7.2.2 Oxidation of 350-nm Silicon Dioxide at 1100°C

This oxide is sufficiently thick to mask the subsequent boron diffusion.

7.2.2.1 The pyrogenic oxidation unit shown in figure 5a is set for the following oxidation schedule:

Oxygen	0.8 L/min	5 min
Oxygen + Hydrogen	0.8 + 0.7 L/min	30 min
Oxygen	0.8 L/min	5 min
Nitrogen	1.0 L/min	15 min

7.2.2.2 Load the wafers into a slotted quartz boat, push the boat to the center zone of the furnace, and initiate the oxidation cycle.

7.2.2.3 At the termination of the oxidation cycle, the wafers are pulled quickly from the furnace and are ready for the photolithographic operation.

7.3 Boron Base Diffusion

7.3.1 Photolithographic Process for Base Diffusion

7.3.1.1 Assure that the silicon wafers are at room temperature by allowing sufficient time for the wafers to cool after removal from the furnace. Place each wafer on the spinner chuck and apply photoresist across the entire exposed surface of the wafer. The photoresist is dispensed from a hypodermic syringe through an inert filter with a pore size of 1.5 μm.

7.3.1.2 Spin the wafer at 4000 revolutions per minute for a period of 15 s.

7.3.1.3 Prebake the wafers at 75°C in an oven for 20 min in nitrogen.

7.3.1.4 Using a base mask in intimate contact with the wafer, expose the wafers for 12 s under an ultraviolet lamp with an intensity of 2230 $\mu W/cm^2$ through the base mask.

7.3.1.5 Develop the photoresist for 20 s in a liquid developer. During the development, gently agitate the wafers to remove the exposed photoresist into the solution.

7.3.1.6 Wash wafers in overflow wash tank for 5 min.

7.3.1.7 Spin wafers dry in a dry nitrogen ambient for 2 min.

7.3.1.8 Post-bake photoresist film at 120°C for 20 min in an air circulating oven.

7.3.1.9 Remove the wafers from the oven and allow to cool at room temperature.

7.3.2 Base Window Etch

7.3.2.1 Etch unprotected silicon dioxide in buffered hydrofluoric acid etch for approximately 2 min. This should be sufficient to completely remove the silicon dioxide layer. The exact time for oxide etching will depend on room temperature and etch strength. Buffered hydrofluoric acid etch is available from chemical manufacturers and consists of a solution of hydrofluoric acid and ammonium fluoride.

7.3.2.2 Wash wafers in an overflow wash tank for 10 min.

7.3.2.3 Inspect wafers under a microscope to ensure complete etching of the pattern through the oxide.

7.3.2.4 If oxide is not completely etched, return wafers to etchant for 30 s. Continue to etch and wash wafers, as described in 7.3.2.1 and 7.3.2.2 until oxide is completely removed.

7.3.2.5 Immerse wafers for 30 s in acetone with gentle agitation to remove all resist and residue.

7.3.2.6 Wash wafers in overflow wash tank for 5 min to remove acetone.

7.3.2.7 Clean wafers, using the same procedure as described in the initial silicon wafer cleaning in section 7.2.1, above.

7.3.3 Boron Base Deposition

7.3.3.1 Adjust the temperature of the diffusion tube to 965°C.

7.3.3.2 Load the silicon wafers into the quartz boat with the boron nitride wafers. The patterned surface of each silicon wafer shall face a boron nitride wafer.

7.3.3.3 Adjust the nitrogen flow in the diffusion tube to 0.5 L/min.

7.3.3.4 Push the wafers into the center of the furnace tube. The diffusion time is approximately 30 min. The time required for the boat to reach the center of the hot zone of the furnace tube is approximately 0.5 min. The diffusion time is approximately 30 min and the withdrawal time is 0.5 min. This diffusion schedule yields a sheet resistance of approximately 70 Ω/□ and a junction depth of 0.4 μm.

7.3.4 Removal of Borosilicate Glass

7.3.4.1 Dip wafers into a solution of 10-percent hydrofluoric acid for 60 s.

7.3.4.2 Rinse wafers in high purity water and spin dry in nitrogen.

7.3.5 Base Drive-in Diffusion and Oxidation at 1100°C

7.3.5.1 Set the pyrogenic oxidation unit for the following schedule:

Oxygen	0.8 L/min	5 min
Oxygen + Hydrogen	0.8 + 0.7 L/min	30 min
Oxygen	0.8 L/min	5 min
Nitrogen	1.0 L/min	60 min

7.3.5.2 Load the wafers into a slotted boat, push the boat into the center zone of the furnace and initiate the oxidation cycle.

7.3.5.3 At the termination of the oxidation cycle, pull the wafers into the neck of the furnace in less than 0.5 min and allow to cool to room temperature. This oxidation produces approximately 350 nm of silicon dioxide over the base regions of the device.

7.4 Phosphorus Emitter Diffusion

7.4.1 Photolithographic Process

A photolithographic process is performed in the same manner as described for the definition of the base diffusion. Coat, bake, align and expose, develop and etch the wafers as described in sections 7.3.1 and 7.3.2, above. The time required to etch the base oxide is approximately 2.5 min.

7.4.2 Phosphorus Diffusion

7.4.2.1 Adjust the emitter diffusion furnace to a temperature of 1025°C. Note that this furnace is not the same furnace used for the boron diffusion.

7.4.2.2 Adjust the nitrogen carrier gas flow to 0.5 L/min through the diffusion tube.

7.4.2.3 Load the silicon wafers to be diffused into the quartz boat with the phosphorus diffusion source wafers. The patterned surface of each silicon wafer shall face a phosphorus diffusion source wafer.

7.4.2.4 Load the wafers into the neck of the diffusion tube and preheat the wafers to a temperature of 350 to 400°C for 10 min. Then push the wafers back into the center zone of the furnace at the rate of approximately 20 cm/min. This prevents the phosphorus wafers from cracking due to thermal shock. Leave the boat in the center zone for approximately 18 min to produce an emitter with a sheet resistance of approximately 10 Ω/□ and a junction depth of 0.8 μm.

7.4.3 Removal of Phosphosilicate Glass

7.4.3.1 Dip wafers into a solution of 10-percent hydrofluoric acid in

water for 10 s to remove the phosphorus-rich oxide grown during the emitter diffusion step.

7.4.3.2 Rinse wafers in an overflow tank of deionized water for 10 min and spin wafers dry in a nitrogen ambient for 2 min.

7.4.4 Emitter Oxidation and Diffusion

7.4.4.1 Load the silicon wafers into a slotted quartz boat and push the boat into the center zone of the furnace.

7.4.4.2 Reoxidize and diffuse the emitter at 925°C according to the following schedule:

Oxygen + Steam	1.0 L/min	30 min
Oxygen	1.0 L/min	5 min
Nitrogen	1.0 L/min	15 min

7.4.4.3 At the end of the oxidation schedule, the emitter junction depth should be about 1.0 μm and the sheet resistance of the emitter should be approximately 15 Ω/□.

7.5 Contact Window Etch

7.5.1 Photolithographic Process

Perform the photolithographic process in the same manner as described for the definition of the base diffusion in section 7.3.1 and 7.3.2, above. The time required for the etching of the contact holes is approximately 2 min. Coat, bake, align and expose, and develop the wafers in the same manner as described before. After the photolithographic operation, clean the wafers to remove any residual photoresist. The wafers are metallized within one hour after the contact window etch.

7.6 Metallization

7.6.1 Evaporate 800 ± 10 nm of aluminum onto the surface of the silicon at a rate of 5 nm/s.

7.6.2 Pattern the aluminum using the same photolithographic process used to pattern the oxides with the exception that the etchant is different. Etch the aluminum metallization in a solution of one part nitric acid, 5 parts high purity water, and 20 parts phosphoric acid. The time required for etching 800 μm of aluminum is approximately 10 min.

7.7 Back Surface Contact

7.7.1 To allow electrical contact to be made to the back surface of the silicon wafer, gold is evaporated on this surface.

7.7.1.1 Place the back surface of the wafer over a cup containing hydrofluoric acid to vapor etch the silicon dioxide. The cup is designed with a flat rim whose diameter is 3 mm less than the diameter of the wafer. The contact between the back surface of the wafer and the rim prevents the fumes from the acid from reaching the front surface which contains the patterned diffusions and metallization.

7.7.1.2 Rinse the wafers in high purity water for 5 min and spin dry in nitrogen.

7.7.1.3 Immediately load the wafers into a vacuum system and coat the back surfaces of the wafers with 100 nm of antimony-doped (0.6%) gold. Use an alumina-coated tungsten-wire crucible charged with the doped gold in the evaporator. Typical current through the tungsten heater is approximately 40 A for an evaporation rate of 50 nm/min.

7.8 Post-Metallization Microalloy

7.8.1 Purpose of Microalloying

The purpose of this step is to microalloy the aluminum and gold metallizations into the silicon to insure the lowest possible contact resistance between the silicon and the metal.

7.8.1.1 Adjust the temperature of the microalloy furnace to 500°C.

7.8.1.2 Adjust the flow of nitrogen at 1.0 L/min. The nitrogen is passed through a cold trap at 77 K immediately prior to its introduction to the furnace to assure a moisture content of less than 10 parts per million.

7.8.1.3 Microalloy the wafers for 10 min.

7.9 Testing

Test the device to determine the sheet resistances, the contact resistances, the transistor gains, and other parameters that reflect the processing steps. The common-emitter current gain of the transistors is measured by plotting the transfer characteristics of the devices on a curve tracer [16]. Figures 8 and 9 show characteristics of a small geometry transistor for values of 1 and 10 microamperes of base current, respectively. Figure 10 is a representation of the inverse current transfer ratio. This is the characteristic formed with the collector and emitter leads interchanged. The base-emitter breakdown voltage is typically 6 V and the base-collector breakdown greater than 70 V.

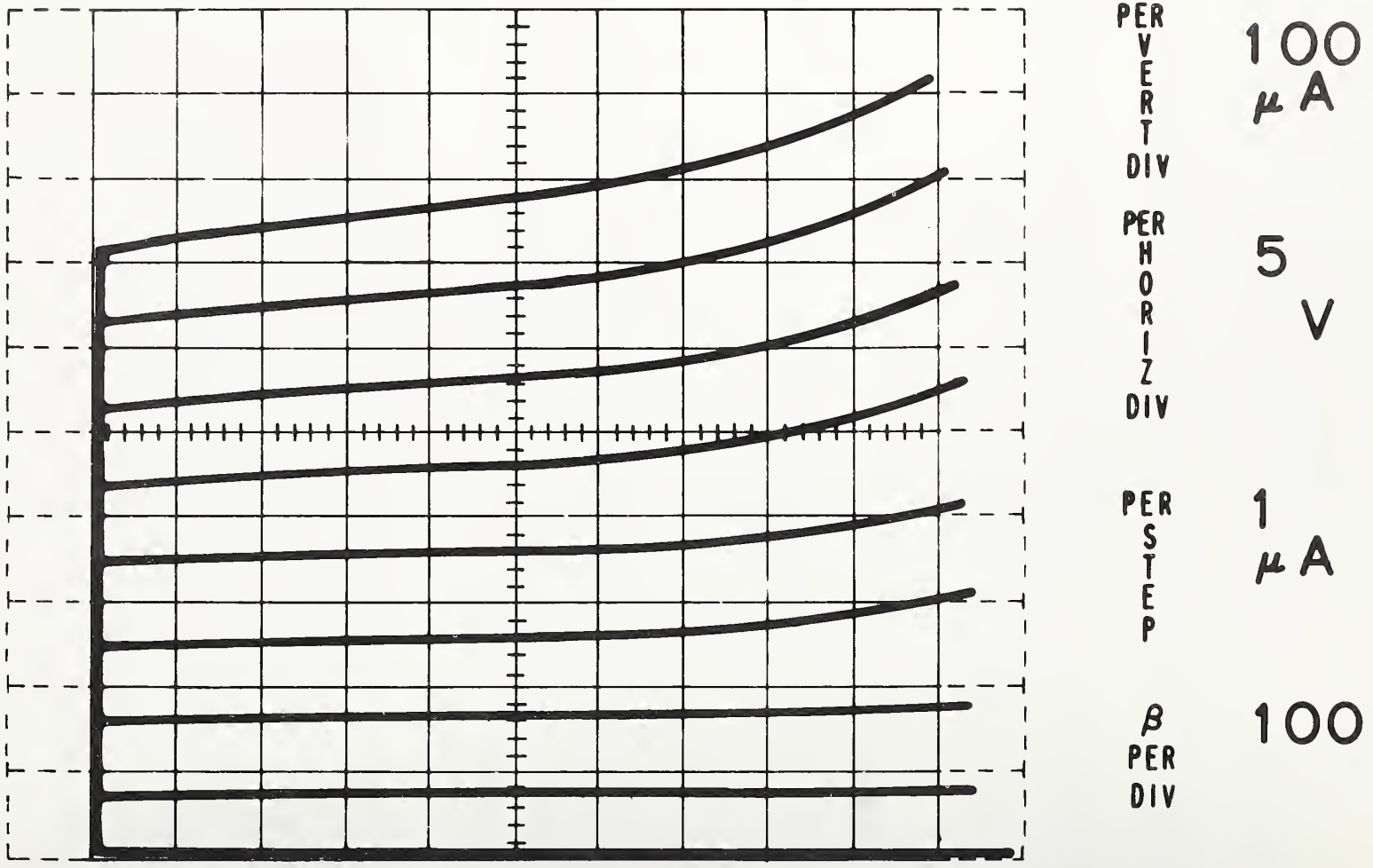


Figure 8. The common-emitter current gain characteristic of the *npn* transistors for 1 microampere/step base current as displayed on a curve tracer.

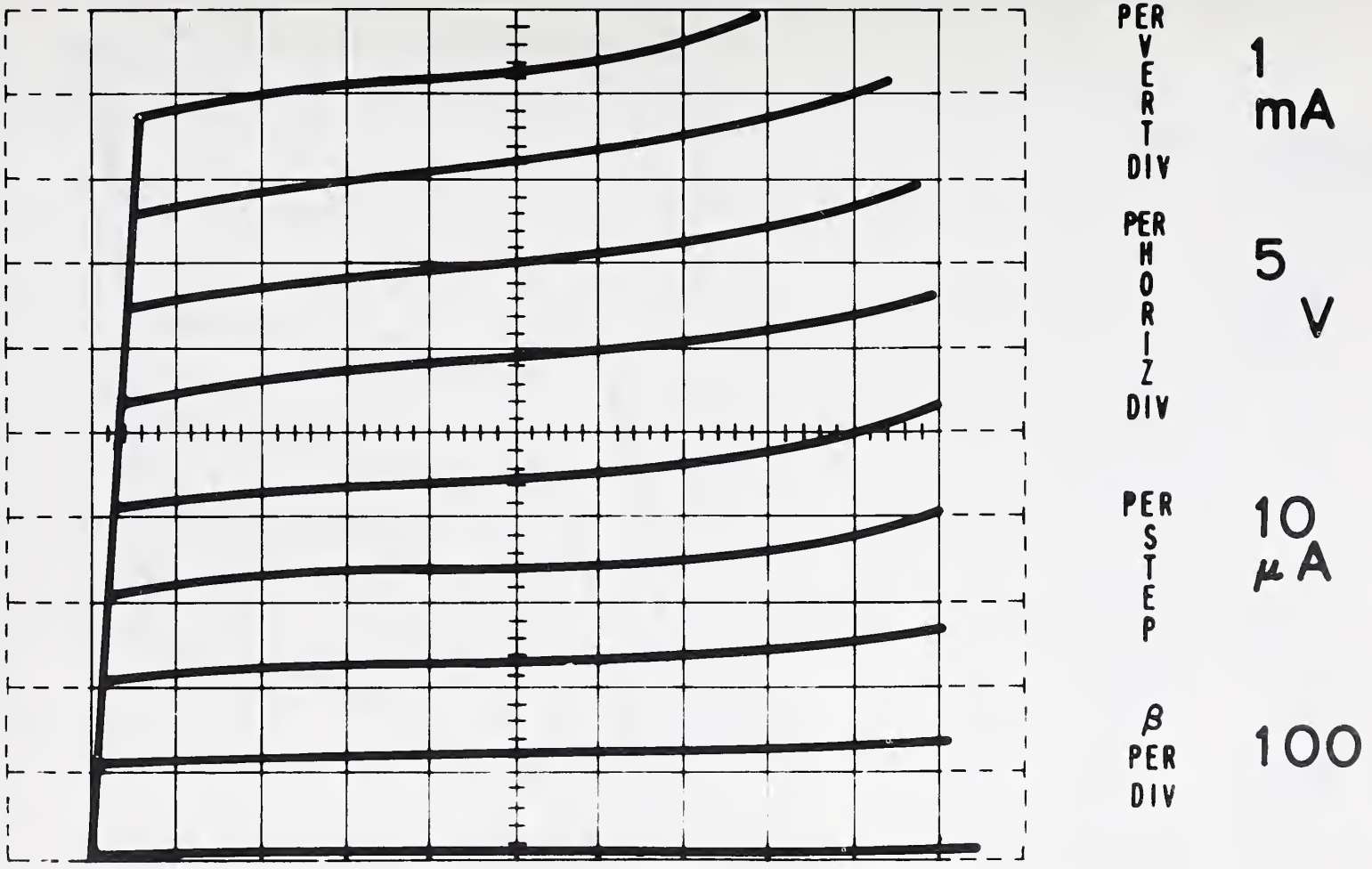


Figure 9. The common-emitter current gain characteristic of the *npn* transistors for a 10 microampere/step base current as displayed on a curve tracer.

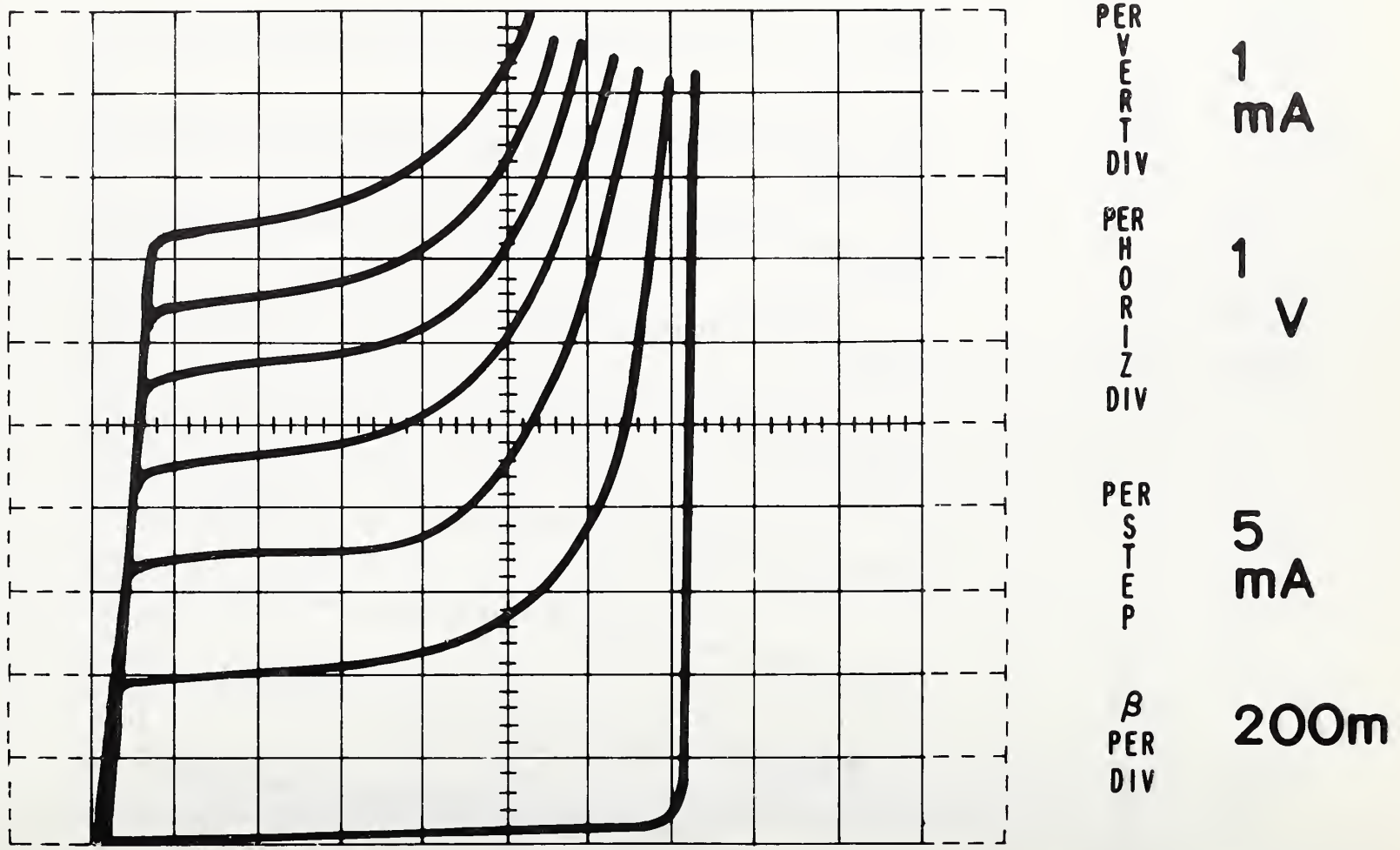


Figure 10. The inverse current transfer characteristic of the *npn* transistors as displayed on a curve tracer.

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This report describes the facilities and processes used at NBS for the fabrication of *npn* silicon transistors in support of the Electron Devices Division's program in process control and measurement technology. The description of the processes includes details of techniques used for contamination control and the various steps required for the preparation of planar silicon transistors. A description of the electrical properties of the devices is also presented.

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